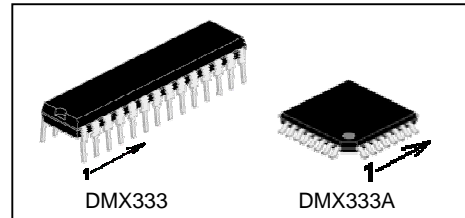


FEATURES

- 5V SUPPLY VOLTAGE
- RECEIVE DMX512 SIGNAL
- 3 PWM OUTPUTS
- 3 ADDITIONAL DIGITAL OUTPUTS
- HIGH PWM FREQUENCY (31,25kHz)
- SYNCHRON SIGNAL DECODING (SSD)
- CASCADEABLE FOR MORE OUTPUTS
- PACKAGE: DIL28S / TQFP32 (RoHS compliant)

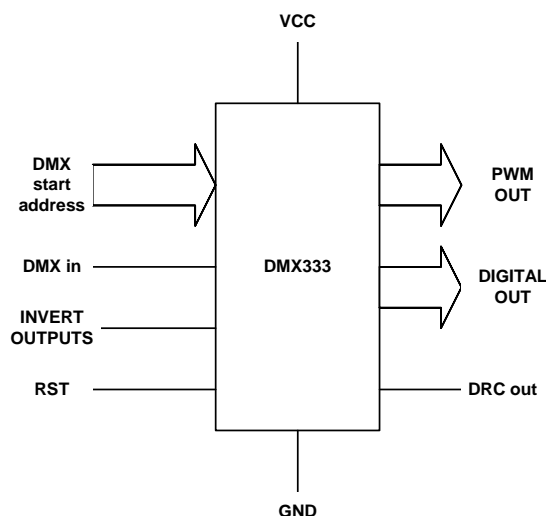


DESCRIPTION

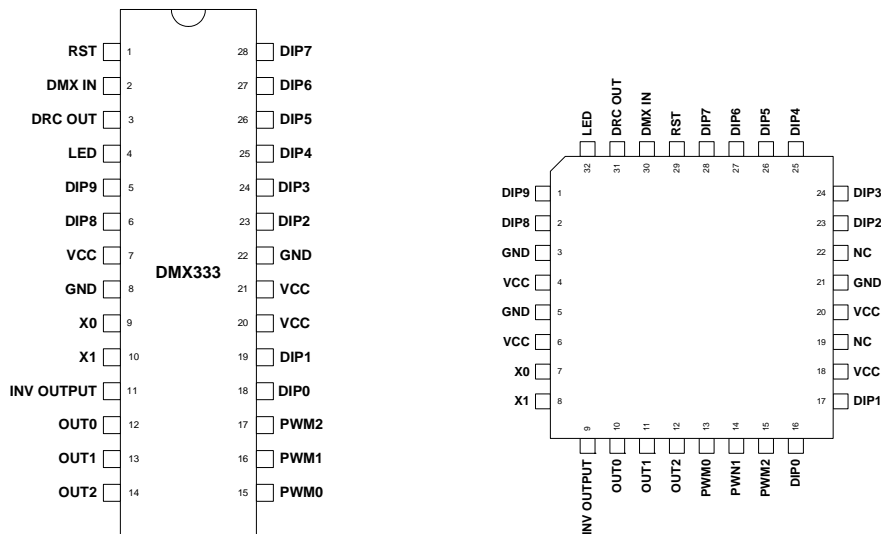
The DMX333 is an DMX512 receiver with three PWM outputs and three additional digital outputs. The received DMX values are buffered to change the outputs synchron for each DMX address (SSD). The PWM waveform is controlled by the level of the received DMX channels.

To combine some DMX333 chips, connect the DRC (DMX Receiver Chain) output with the DMX input from the next chip. The synchron output change is not supported in this case. More informations about the DRC you can find in the separate document.

LOGIC SYMBOL



PIN CONFIGURATION



PIN DESCRIPTION

MNEMONIC	PIN (DIL28S)	PIN (TQFP32)	TYPE	NAME AND FUNCTION
RST	1	29	I	RESET Reset input. A low level on this pin for more then 50ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset
DMX IN	2	30	I	DMX-SIGNAL Input for the DMX512 signal
DRC OUT	3	31	O	DRC-SIGNAL Output for the DRC signal
VCC	7;20;21	4;6;18;20	I	POWER This is the power supply
GND	8;22	3;5;21	I	GROUND 0V reference
X0	9	7	I	XTAL0 Input from the inverting oscillator amplifier
X1	10	8	O	XTAL1 Output from the inverting oscillator amplifier
LED	4	32	O	STATUS LED LED output. This pin can sink 20mA to drive a LED
PWM0,1,2	15;16;17	13;14;15	O	DIGITAL PWM OUTPUT Output for the PWM signal controlled by DMX value
DIP0-8	18;19;23 24;25;26 27;28;6	16;17;23 24;25;26 27;28;2	I	ADDRESS INPUT Input for the DMX start address
DIP9	5	1	I	RESERVED INPUT This pin is without function.
INV OUTPUT	11	9	I	INVERT OUTPUTS If this pin is LOW, the outputs are all inverted.
OUT0-2	12;13;14	10;11;12	O	DIGITAL OUTPUT Output controlled by DMX value
NC		19,22		NOT CONNECTED

ELECTRICAL CHARACTERISTICS

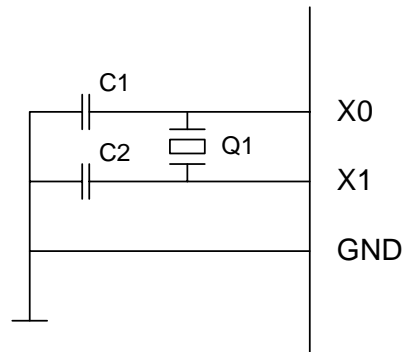
Parameter	Description	Min	Typ	Max	Units	Conditions
VCC	Operating Supply Voltage	3,5	5	5,5	V	
ICC	Operating Supply Current				mA	
VIH1	Input High Voltage	0,6		VCC+0,5	V	
VIH2	Input High Voltage	0,9		VCC+0,5	V	RESET Pin
VIL	Input Low Voltage	-0,5		0,2	V	
fOSZ	Oszillator Frequency		8		MHz	
fPWM	PWM Frequency		31,25		kHz	

Absolute Maximum Ratings

Operating Temperature	-55°C to +125°
Storage Temperature	-65°C to +150°C
Voltage on any Pin except RESET with respect to Ground	-0.5V to VCC+0.5V
Voltage on RESET with respect to Ground	-0.5V to +13.0V
Maximum Operating Voltage	6.0V
DC Current per I/O Pin	40.0 mA
DC Current VCC and GND Pins	200.0 mA

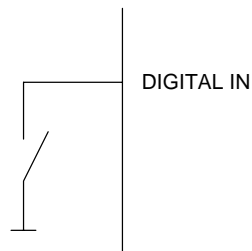
DEVICE CONFIGURATION EXAMPLES

Oscillator Configurations



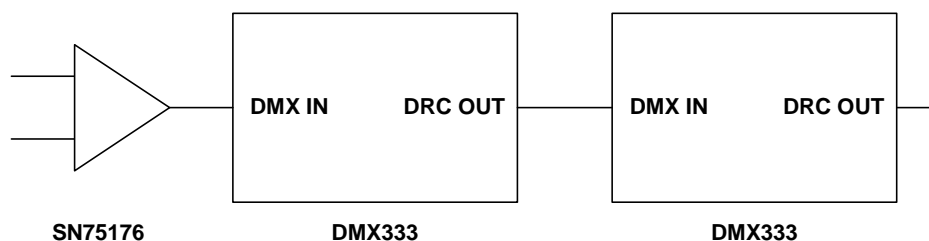
This example illustrates how to use the DMX333 with a 8MHz crystal. The value of the capacitors should be in the range of 12-33pF.

Digital Input Configuration



Some of the pins of the DMX333 used as digital inputs. This pins are connected with a switch to GND.

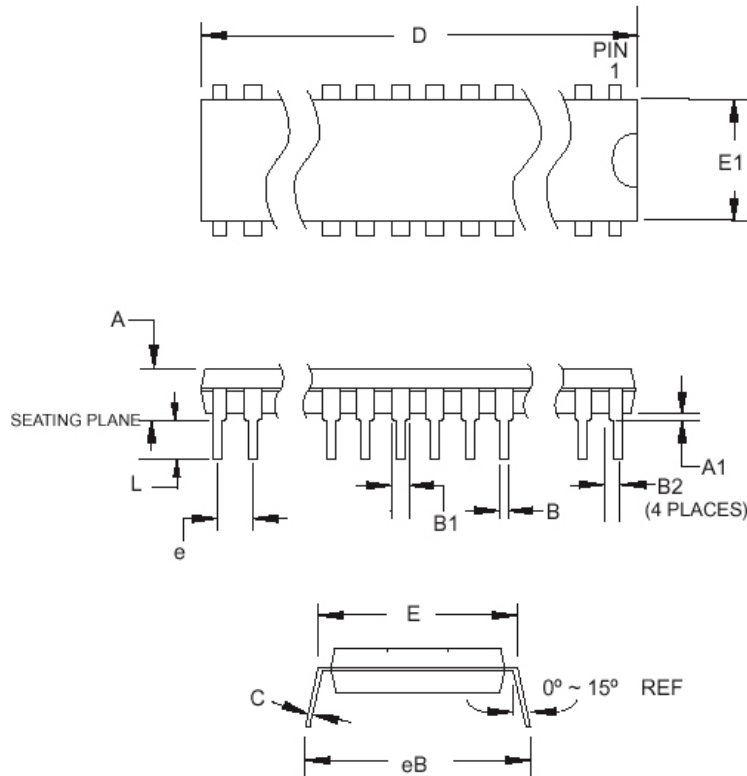
DMX Interface Configuration



The DMX333 is cascadeable, as the DRC exit is connected with the DMX entrance of the next component. The first DMX input receives the signal from the line driver.

PACKAGING INFORMATIONS

DMX333 (DIL28S)

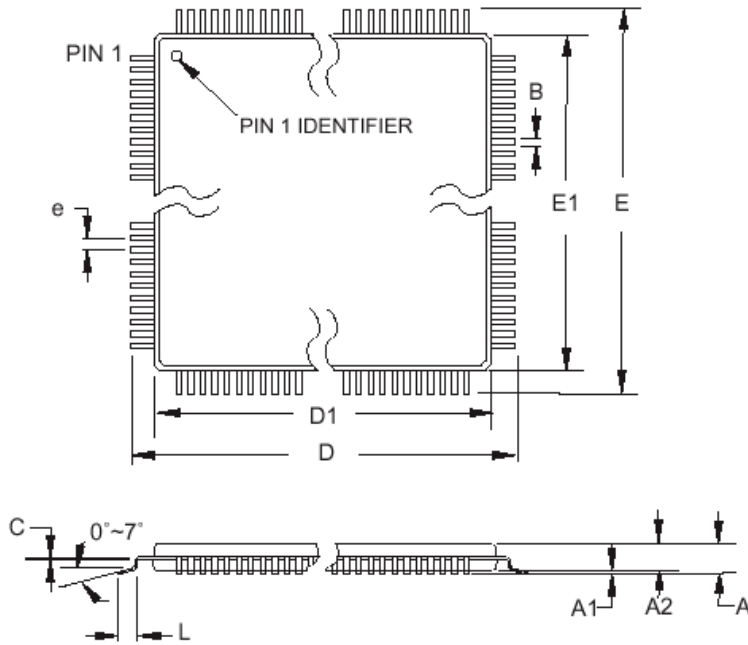


COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	4.5724	
A1	0.508	-	-	
D	34.544	-	34.798	Note 1
E	7.620	-	8.255	
E1	7.112	-	7.493	Note 1
B	0.381	-	0.533	
B1	1.143	-	1.397	
B2	0.762	-	1.143	
L	3.175	-	3.429	
C	0.203	-	0.356	
eB	-	-	10.160	
e	2.540 TYP			

PACKAGING INFORMATIONS

DMX333A (TQFP32)



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	-	0.45	
C	0.09	-	0.20	
L	0.45	-	0.75	
e	0.80 TYP			

1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.



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